EUVL Advancements Toward HVM Readiness

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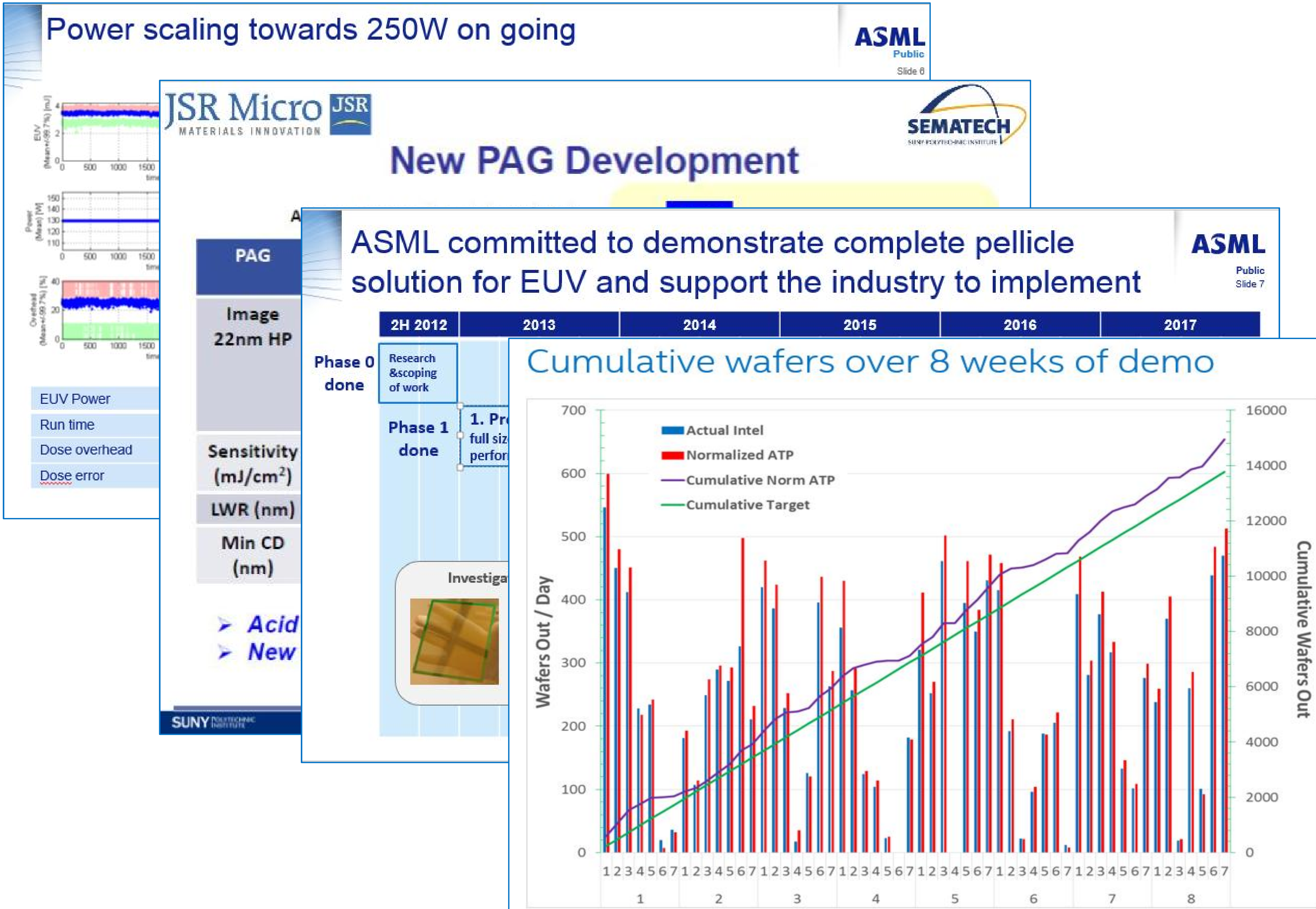
Intel Corporation

“When”, versus “If”…



Outline

- Review EUVL outlook at 2014 Source Workshop
- Recent progress and remaining gaps
- EUVL infrastructure
- Next steps toward production

As of 2014 Source Workshop

Conclusions

- Solid progress in last year, with realization of 40~80W stable MOPA+PP sources in the field
- Availability is not adequate for process development and needs substantial improvement over next two quarters
- *In situ* collector cleaning looks promising, but needs to be delivered to field to gain confidence in OpEx and stable productivity
- Continued progress on source power per roadmap is required to build confidence in long-term productivity targets and COO
- EUV infrastructure is now lagging scanner and source, and needs increased focus

Field system conversions continue

Multiple field systems at 80W

Most field systems in 80W configuration, initially operating at 60W

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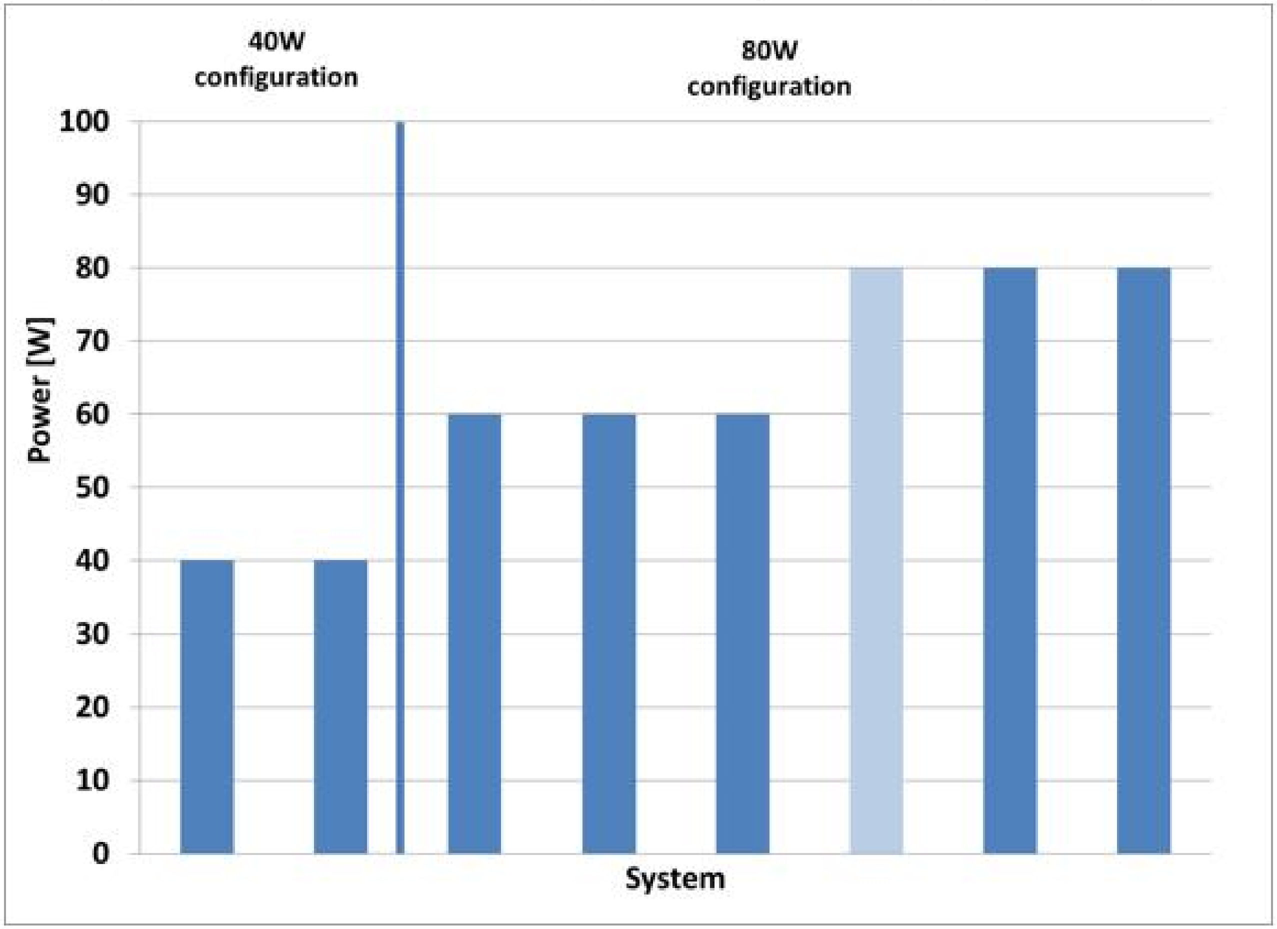
Slide 2

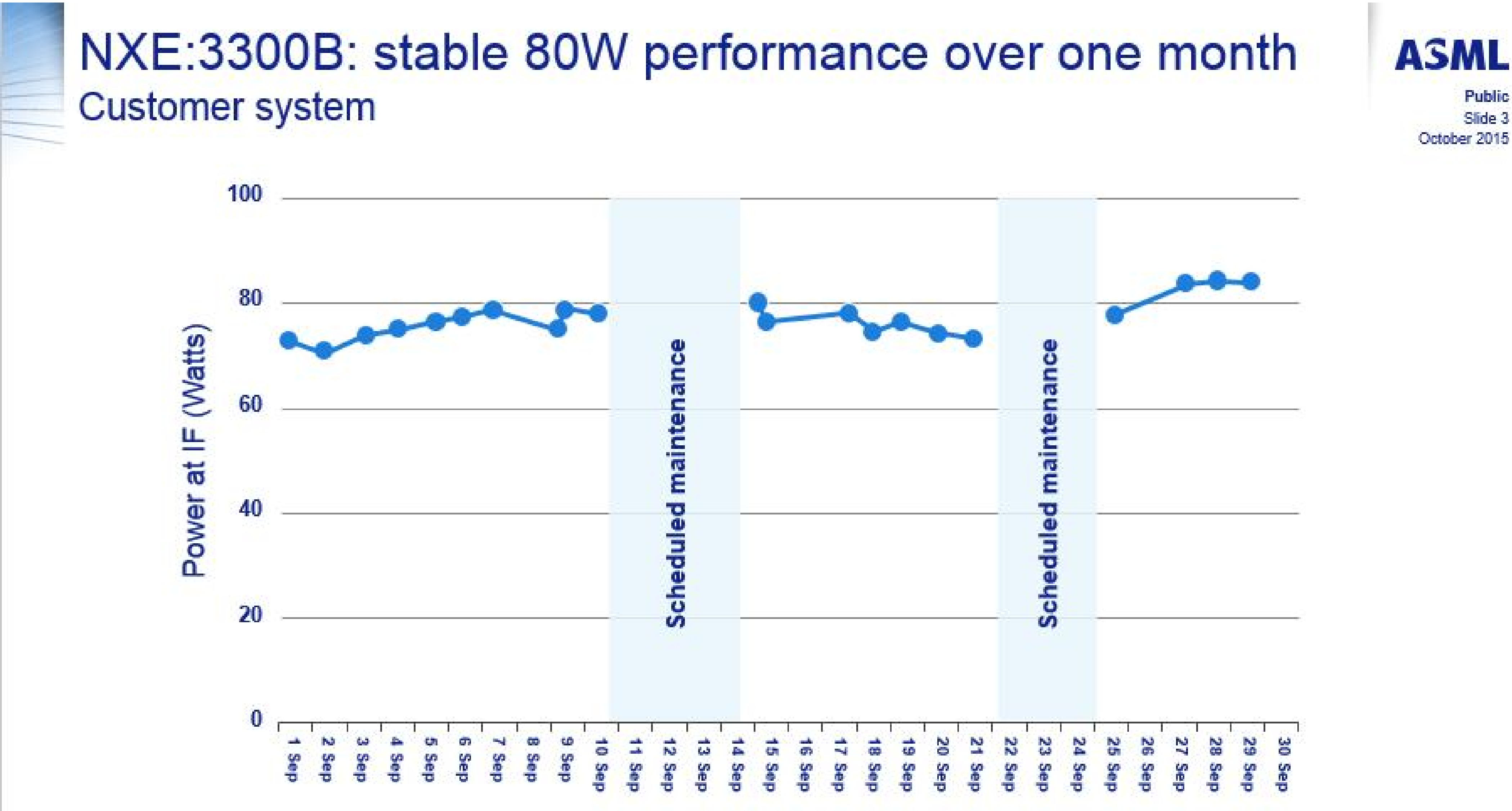


Upgrade on going

Slide courtesy ASML, October 2015

- Solid momentum with 80W conversions; operating power restricted to protect collector: need schedule for collector improvements, including *in situ* collector cleaning, to remain on track

Stable 80W performance in the field



Slide courtesy ASML, October 2015

- System running with collector lifetime improvements demonstrates 80W

Progress in last year: Worldwide summary

- 11 NXE:33x0 systems shipping by end of 2015[1] (7 at this time last year)
- 8 NXE systems in the field with source running >40W[1] (4 at this time last year)
- 5 NXE systems in the field with source in 80W configuration[1] (1 at this time last year)
- >1000 wafers in 24 hours demonstrated at customer site[3] (500 wpd at this time last year)

1. Per John Barbuto (ASML) Nov. 2015
2. Per Jack Chen (TSMC) at 2015 EUVL Symposium

As of 2014 Source Workshop

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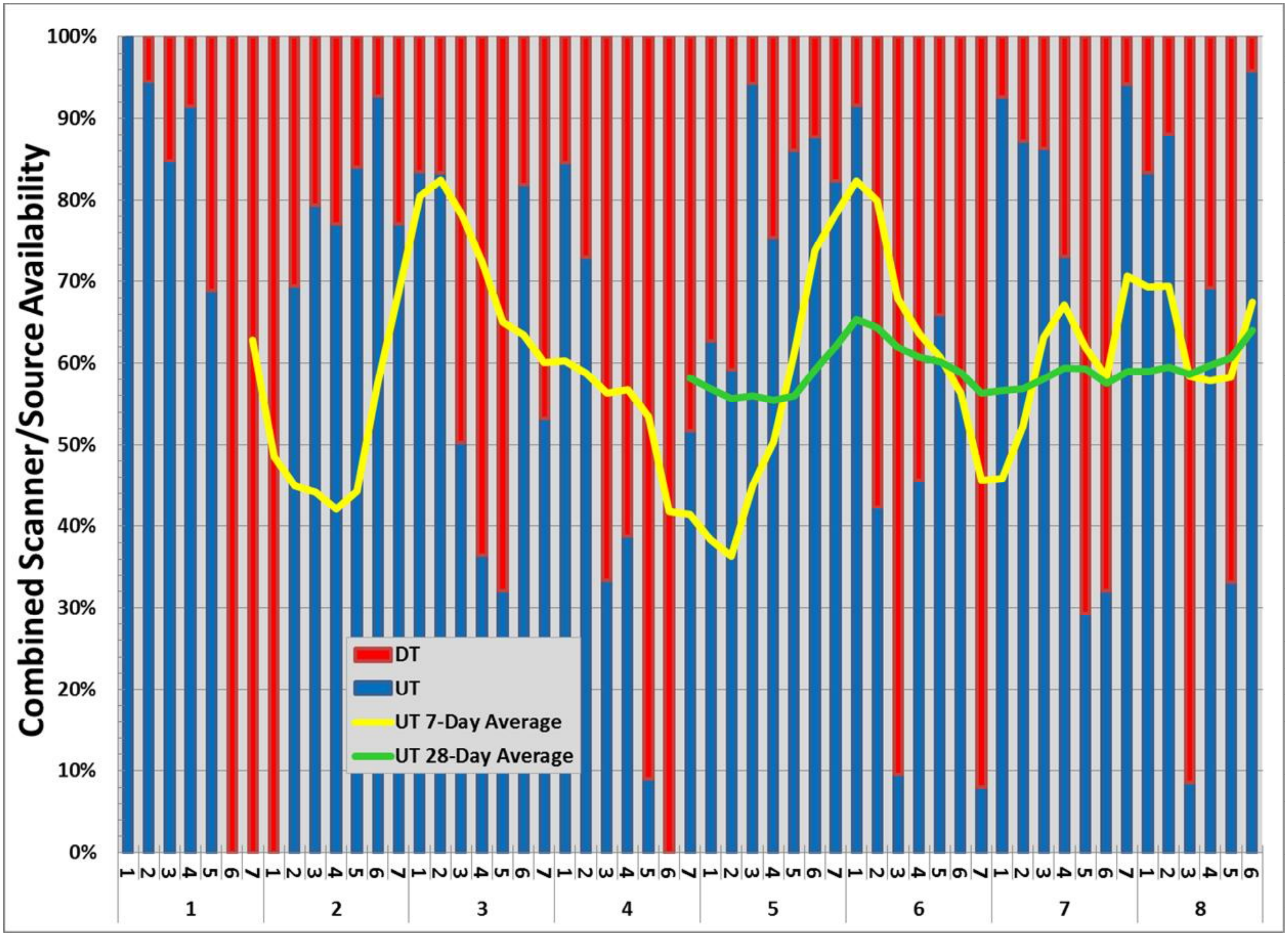
Demo 2: Extended NXE:3300 demo of availability and predictability in 80W config

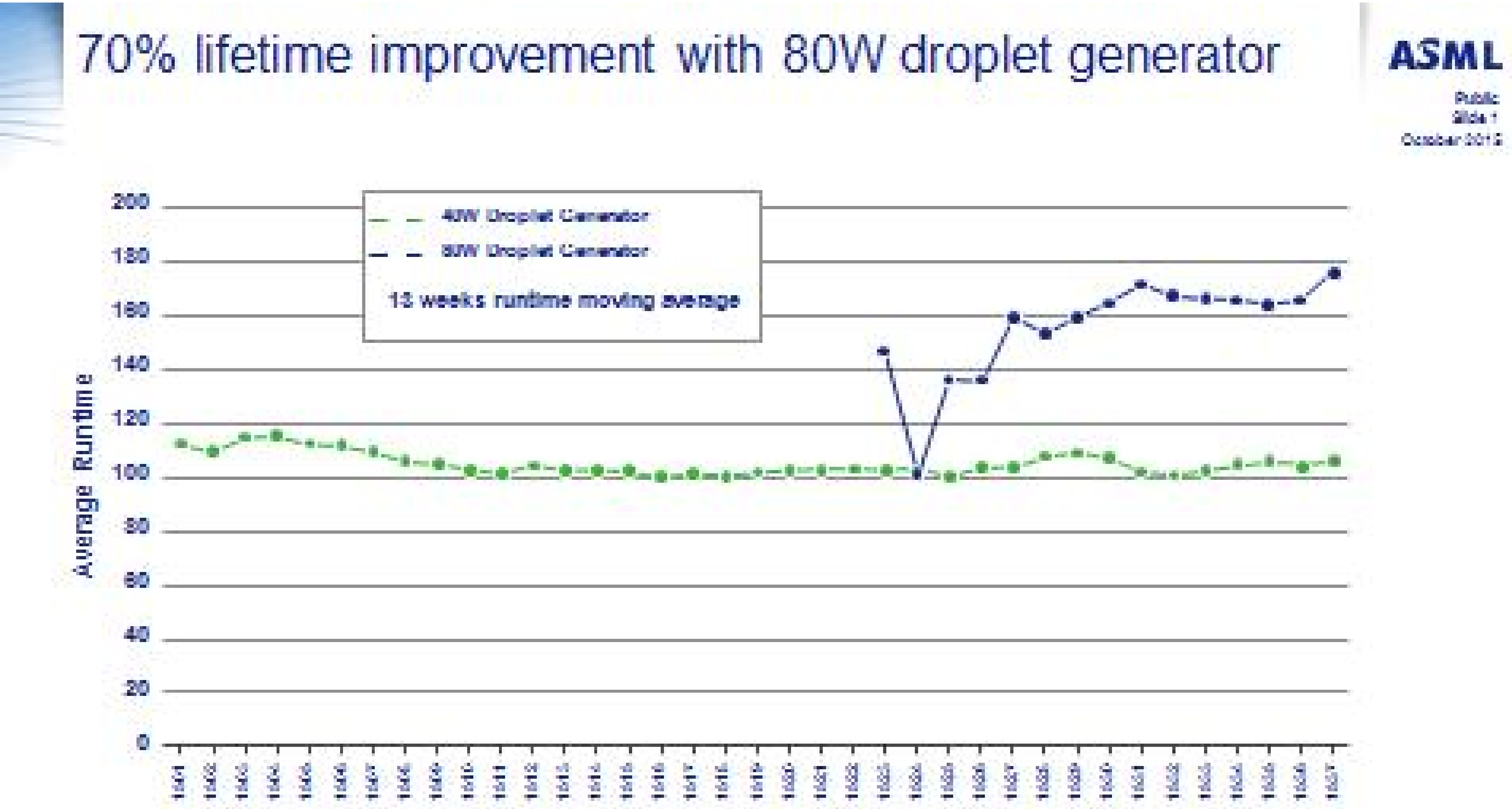
- 21hrs/day wafer cycling with mix of test-chip wafers (CDs, overlay, in-line defects, e-test) and bare silicon
- 3-hr daily Intel engineering window (no tool work)
- Availability counted 24hrs/day. Wafer output targets set for 21hrs/day in 80W config.
- Only good wafers (meeting dose control specs) counted
- Goal: demonstrate tool can run as advertised for 80W config today, *including imaging and overlay*

NXE:3300 combined availability



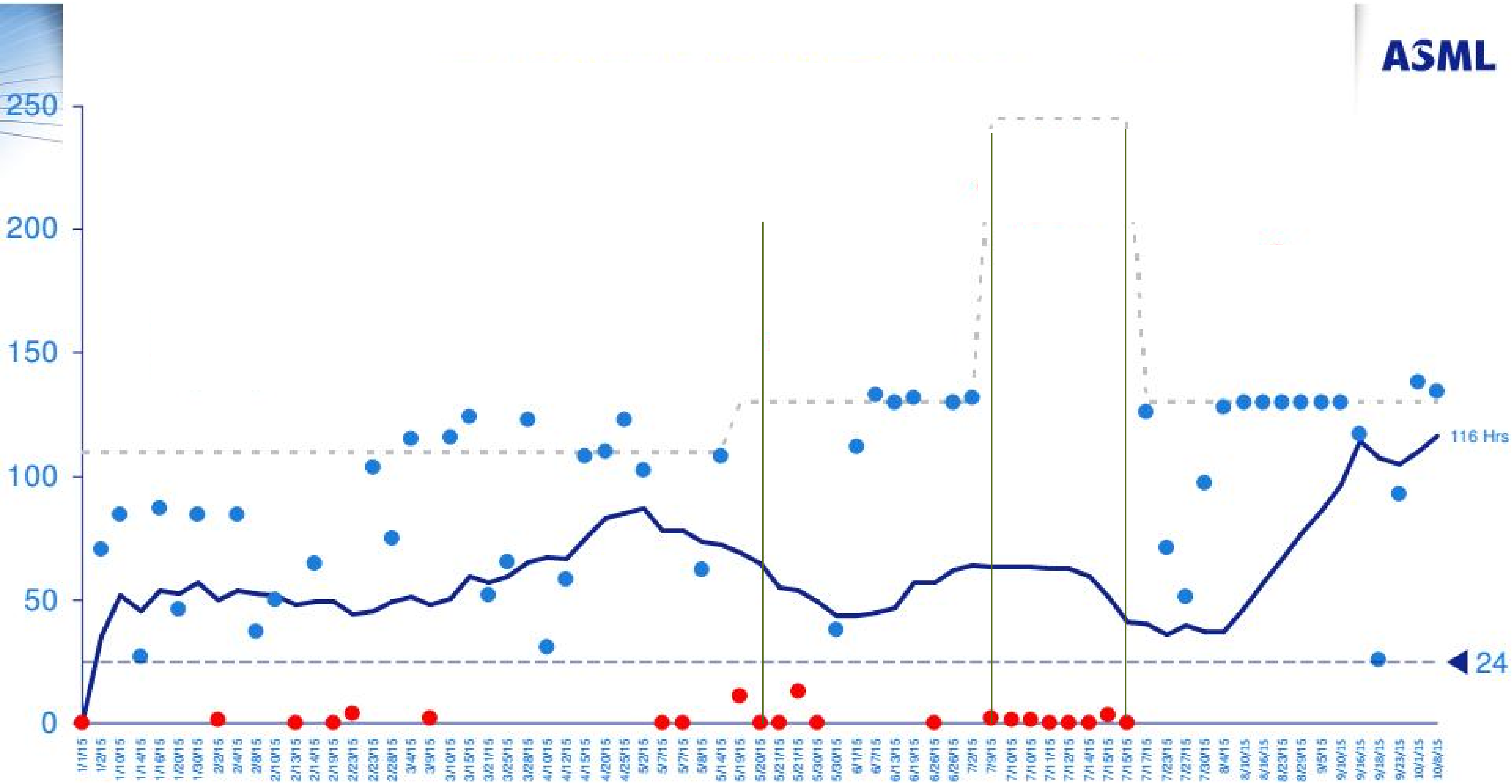
- Source availability is trending toward expectation; combined availability is limited by scanner availability.

DG lifetime



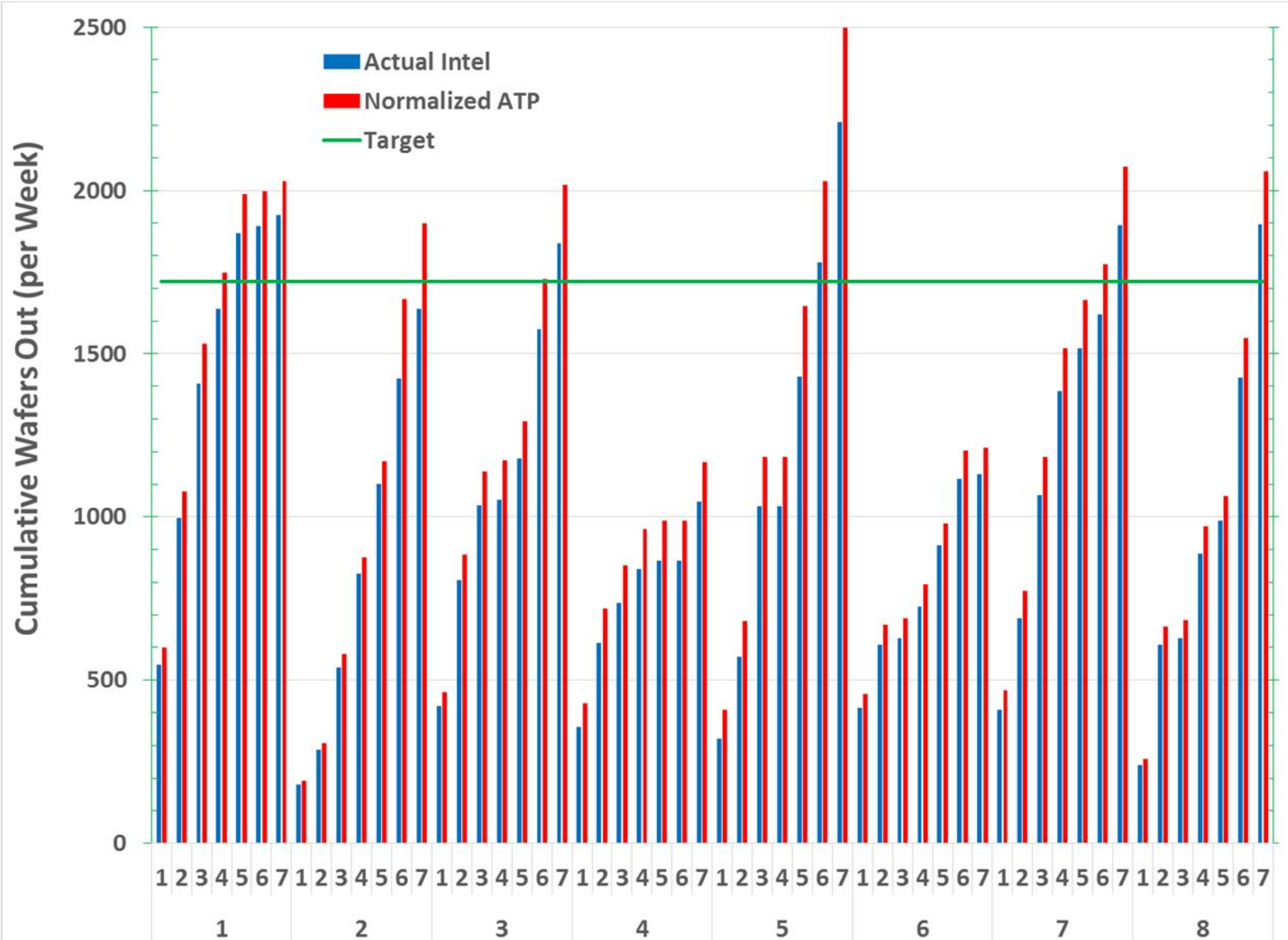
- Significant increase in lifetime with implementation of DG improvements

In-house droplet generator update



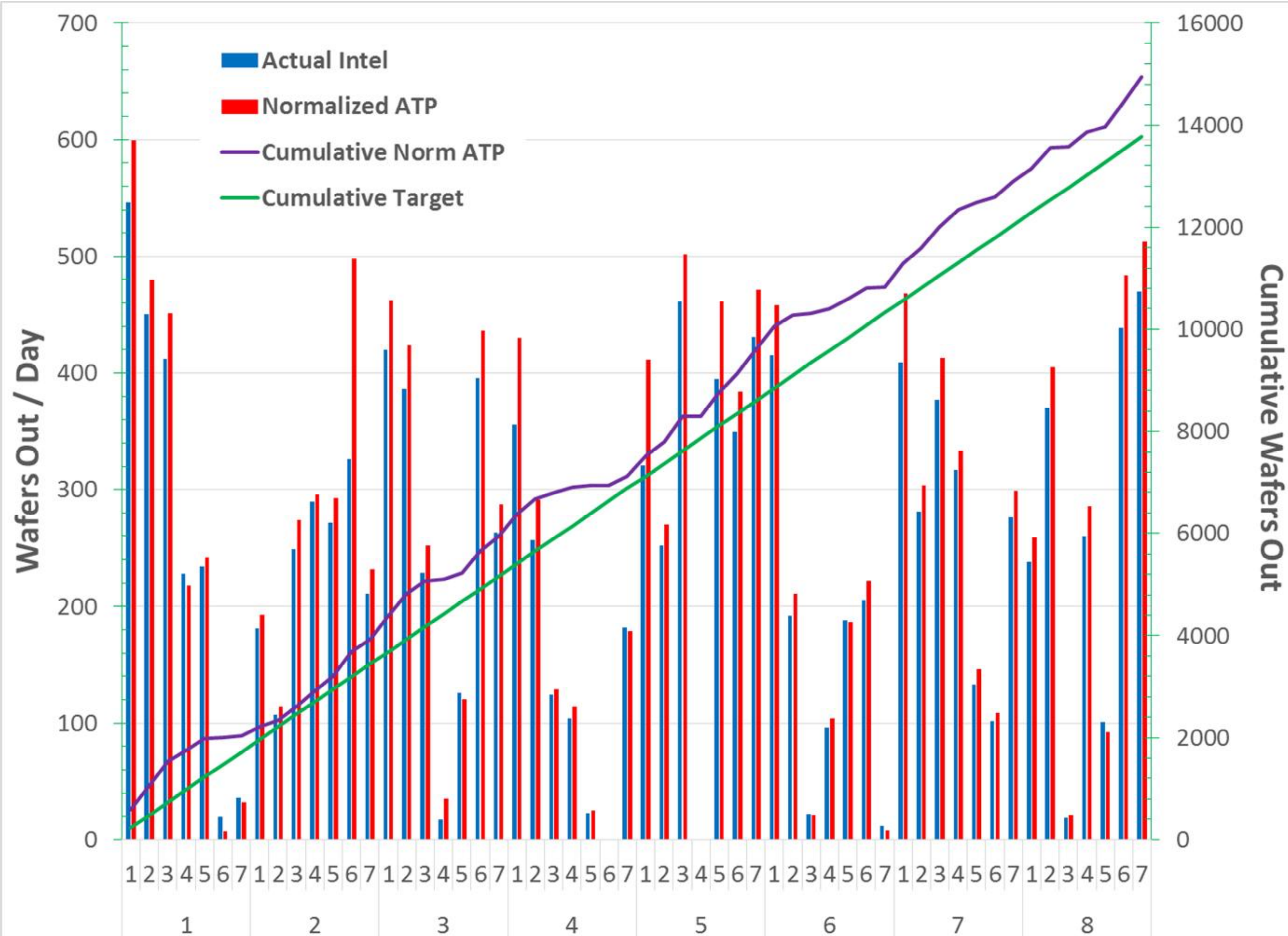
- Significant improvement in DOA rate after initial elevated DOA with implementation of modification

NXE:3300 80W config: cumulative wafers per week



- Weekly outs exceeding goal for six of eight weeks

Cumulative wafers over 8 weeks of demo

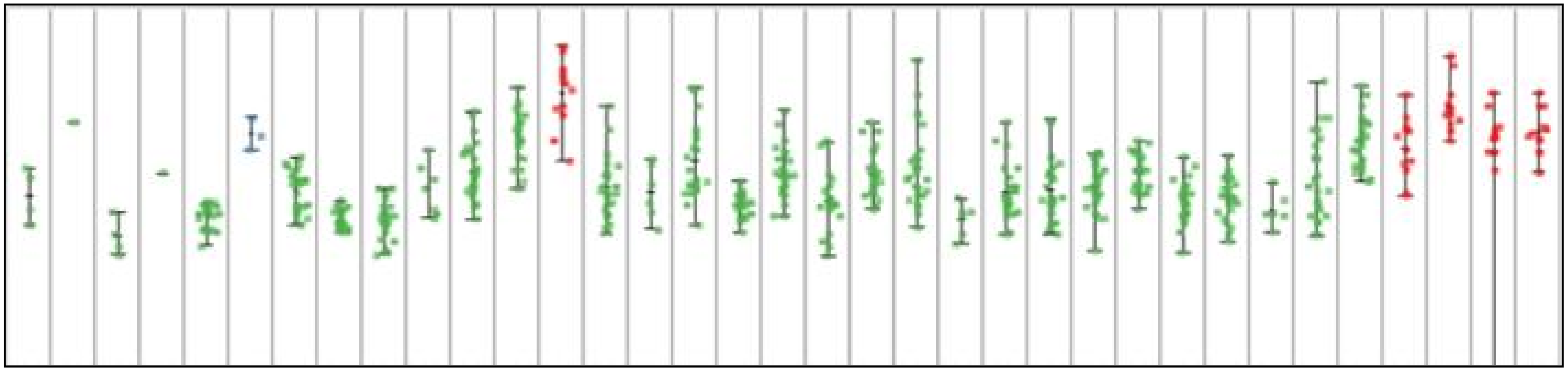


- >15,000 wafers processed during 8-weeks

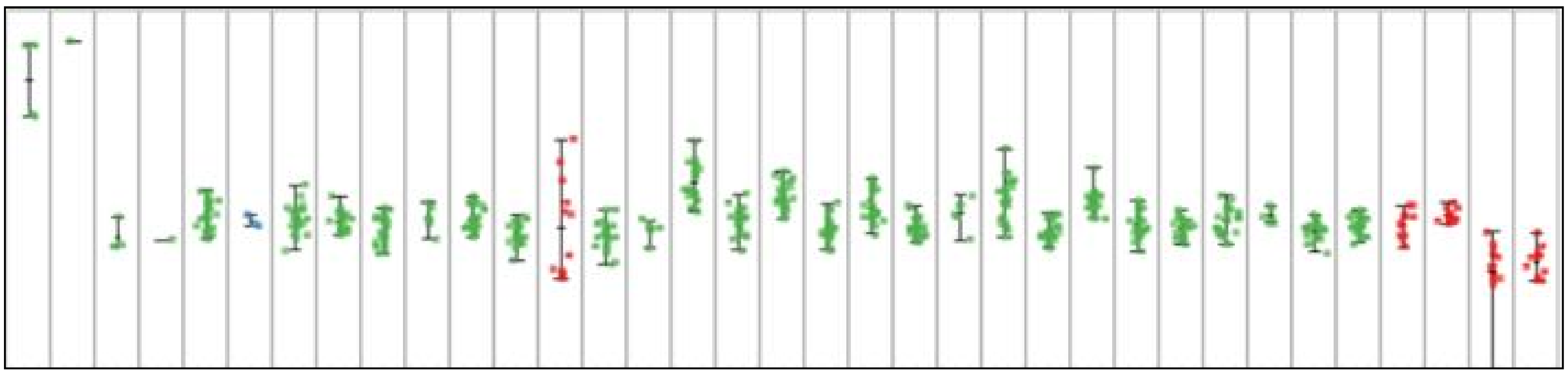
Measured overlay trend

Green = NXE (EUV) to NXT (193i)
Red = NXT to NXT (MMO)

X-max



Y-max



Time (4 weeks), each point is one wafer; each cluster is one lot

- OK. No overlay penalty for EUV-193i versus 193i-193i MMO.

Blue = updated from 2014 Source Workshop

Progress in last year: NXE performance in-house

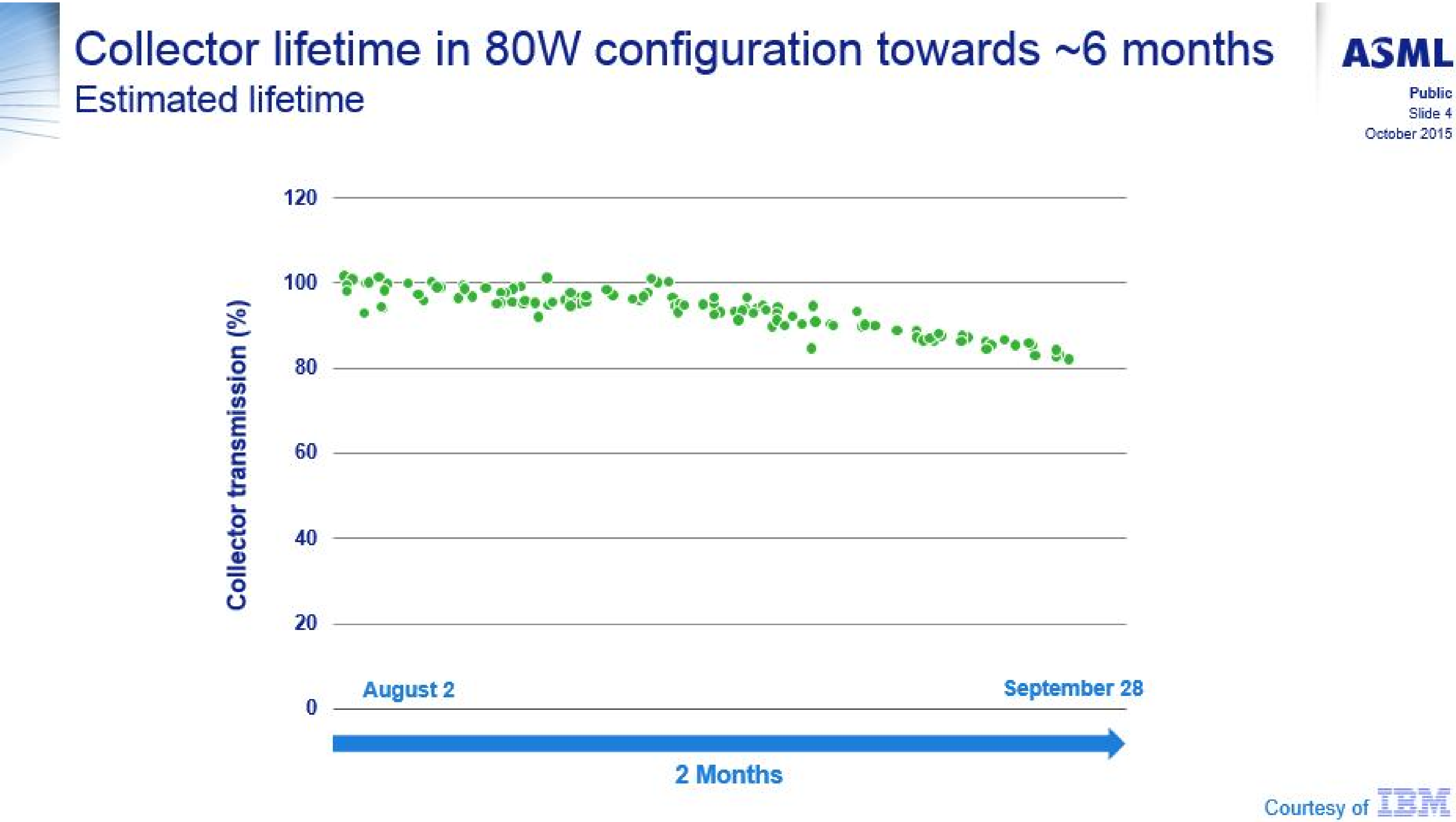
- System (scanner + source) meets all specs except productivity – continues with additional systems
- Productivity is consistent with source power
- Power is stable and dose control is good
- Scanner availability is solid
- Source availability is still poor (average <40%), with Droplet Generator the biggest contributor – availability remains limited by source but trend continues to improve with average ~60%

As of 2014 Source Workshop

Conclusions

- Solid progress in last year, with realization of 40~80W <u>stable</u> MOPA+PP sources in the field Update: stable field performance in 80W config, peak operating power limited to protect collector.
- Availability is not adequate for process development and needs substantial improvement over next two quarters Update: significant gains in availability, largely due to improvements in DG. Need to consistently demonstrate target availability across the fleet.
- *In situ* collector cleaning looks promising, but needs to be delivered to field to gain confidence in OpEx and stable productivity
- Continued progress on source power per roadmap is required to build confidence in long-term productivity targets and COO
- EUV infrastructure is now lagging scanner and source, and needs increased focus

Continuing improvement in collector lifetime



Slide courtesy ASML, October 2015

- Demonstrated improvement in collector lifetime lends credibility to projected lifetime

As of 2014 Source Workshop

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- *In situ* collector cleaning looks promising, but needs to be delivered to field to gain confidence in OpEx and stable productivity Update: collector lifetime improving but limiting operating power. Need collector improvements including *in situ* collector cleaning proliferated to field systems.
- Continued progress on source power per roadmap is required to build confidence in long-term productivity targets and COO
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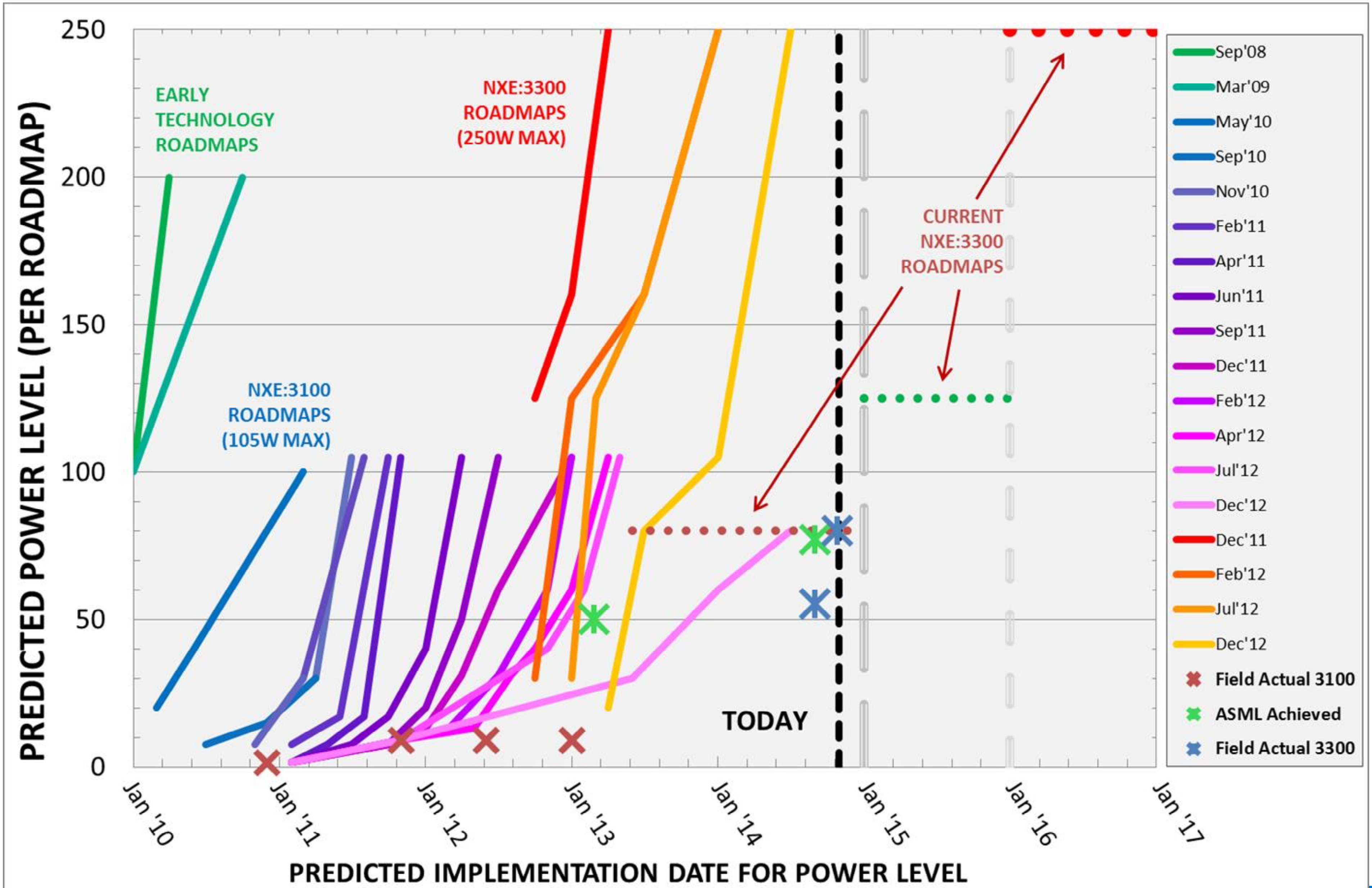
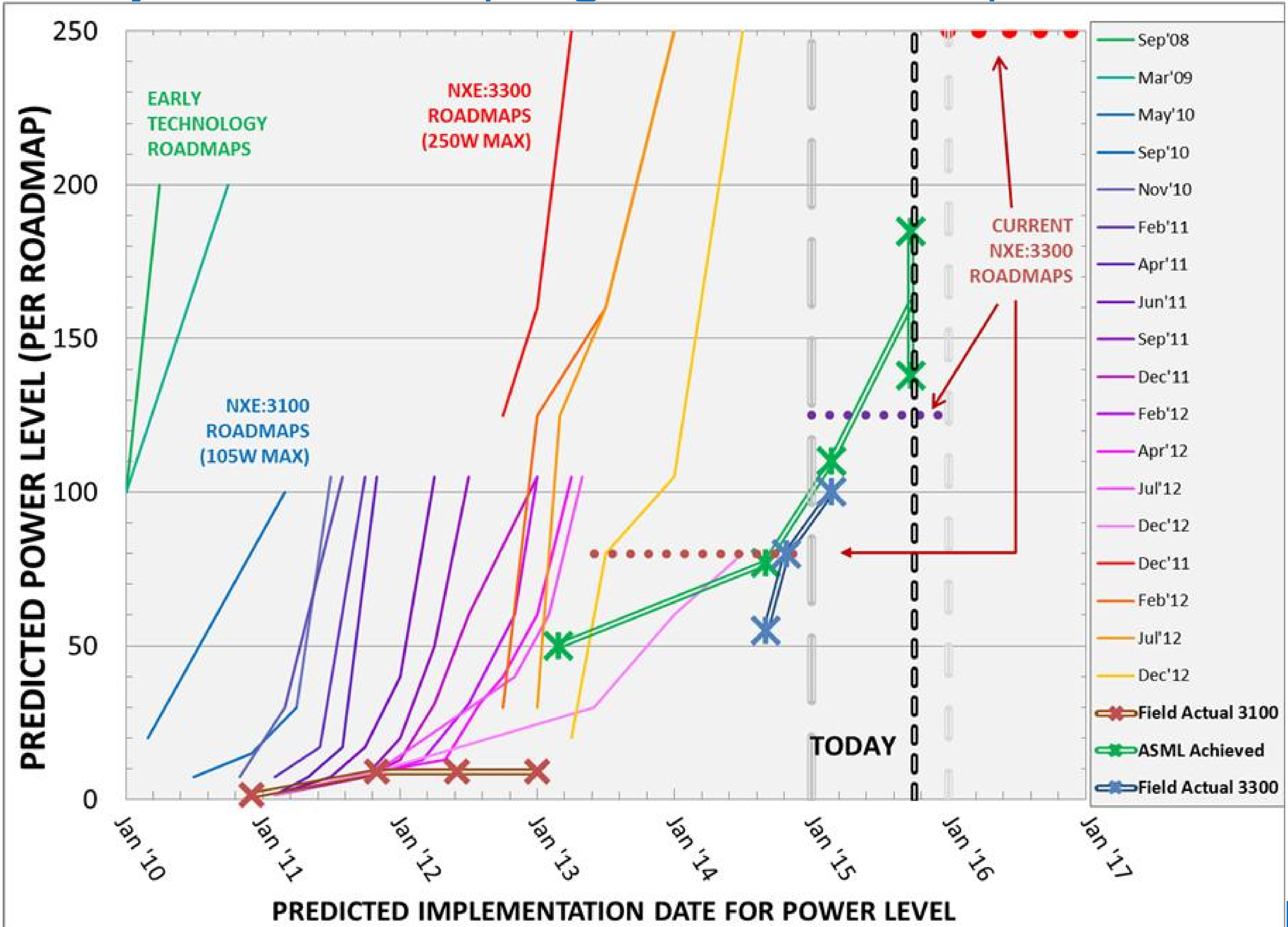
As of 2014 Source Workshop

Source power roadmap is regaining credibility



Today

Two years of solid progress on source power



Demonstrated sustained 95W source power

NXE:3350B: stable 95W performance over 10 days

At ASML factory

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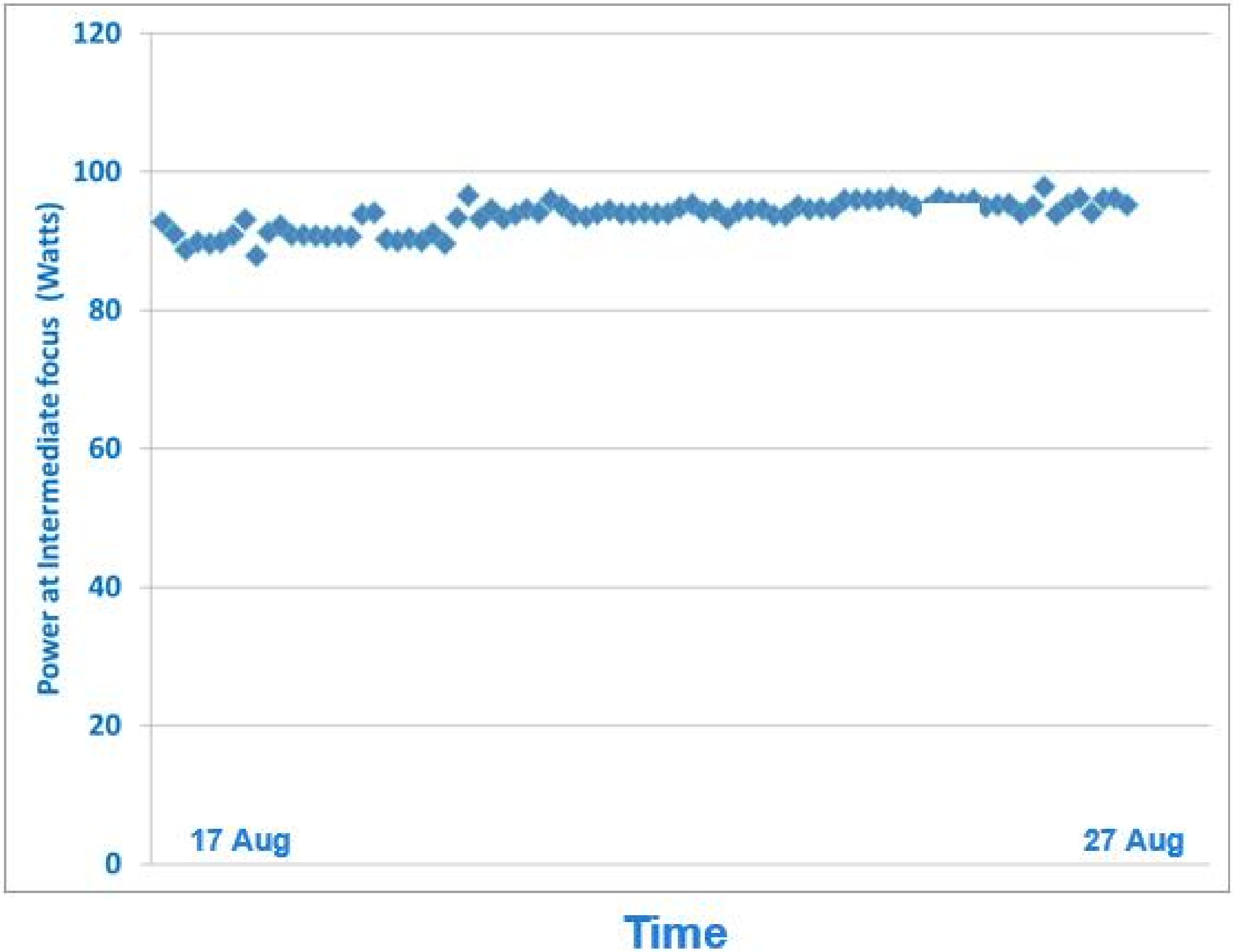
October 2015



Slide courtesy ASML, October 2015

Confidence in reaching 250W

Power scaling towards 250W on going

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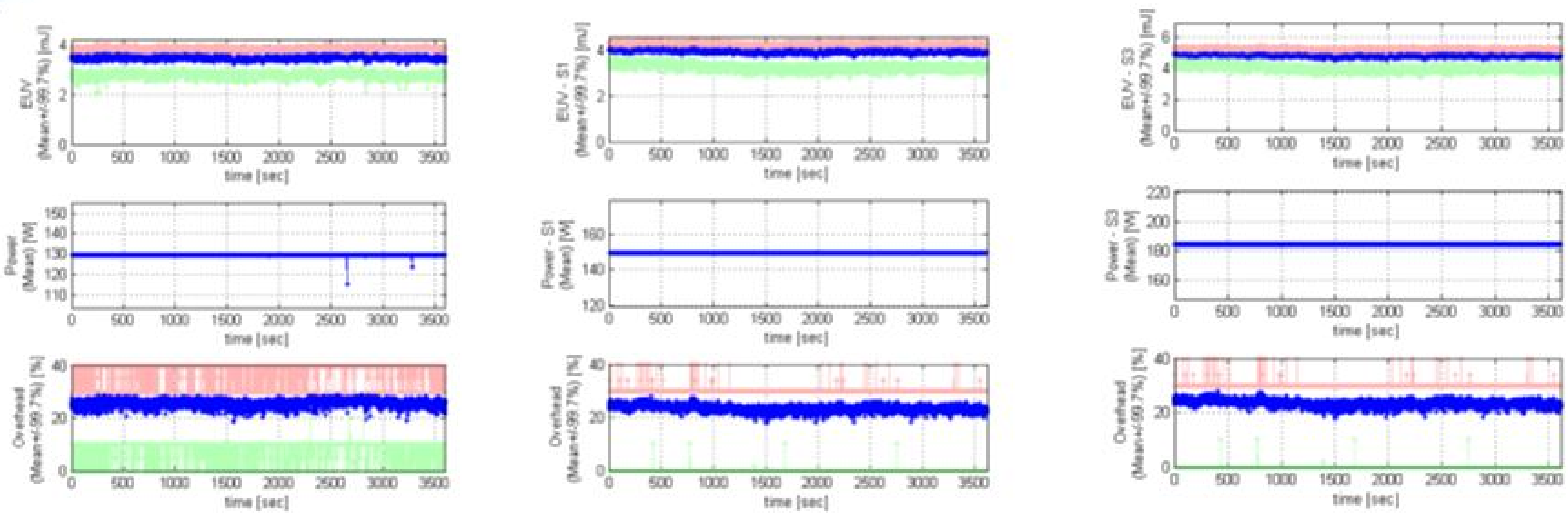

EUV Power	130W
Run time	1 hour
Dose overhead	26%
Dose error	99.9% spec

EUV Power	150W
Run time	1 hour
Dose overhead	23%
Dose error	100% spec

EUV Power	185W
Run time	1 hour
Dose overhead	23%
Dose error	100% spec

Slide courtesy ASML, October 2015

- Subsequent keynote by Wim van der Zande (ASML)

Blue = updated from 2014 Source Workshop

EUV Source Milestones for HVM insertion and beyond

To keep HVM insertion on track:

- Stable availability ~70% (sustained on fleet, not peak) in 1H16
- Proliferation of *in situ* collector cleaning in 1H16, for both COO and stable productivity
- Progress towards 125 & 250W roughly per schedule

For long-term viability:

- Power scaling to ~1kW → ~500W maybe OK given 2X transmission of new optics design
- Maintaining productivity (150 wph at 60mJ/cm^2) with High NA requires continued increase in source power → 500W
- Dramatic improvements in COO

As of 2014 Source Workshop

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- Continued progress on source power per roadmap is required to build confidence in long-term productivity targets and COO Update: >2x increase in source power over the past year lends credibility to source power roadmap. Matching productivity for High-NA requires ~2X increase in source power.
- EUV infrastructure is now lagging scanner and source, and needs increased focus

From 2014 Source Workshop

EUV Infrastructure Readiness Snapshot

EUV infrastructure has 8 key programs

1 is ready now, 4 are in development, 3 have significant gaps

- **E-beam Mask Inspection:** HVM capable tool exists
- **AIMS Mask Inspection:** SEMATECH led tool development program
- **Actinic Blank Inspection (ABI):** EIDEC led tool development program
- **Pellicle:** C&F results demonstrated
- **EUV blank quality:** Process and yield improvements ongoing
- **Actinic Patterned Mask Inspection (APMI):** Required for post-pellicle inspection. Industry development framework definition required.
- **Blank multi-layer deposition tool:** Improving defect results. Multiple deposition techniques being evaluated to define HVM tool approach.
- **EUV resist QC:** Rapid turn resist QC infrastructure definition required

Judged as of Today

EUV Infrastructure Readiness Snapshot

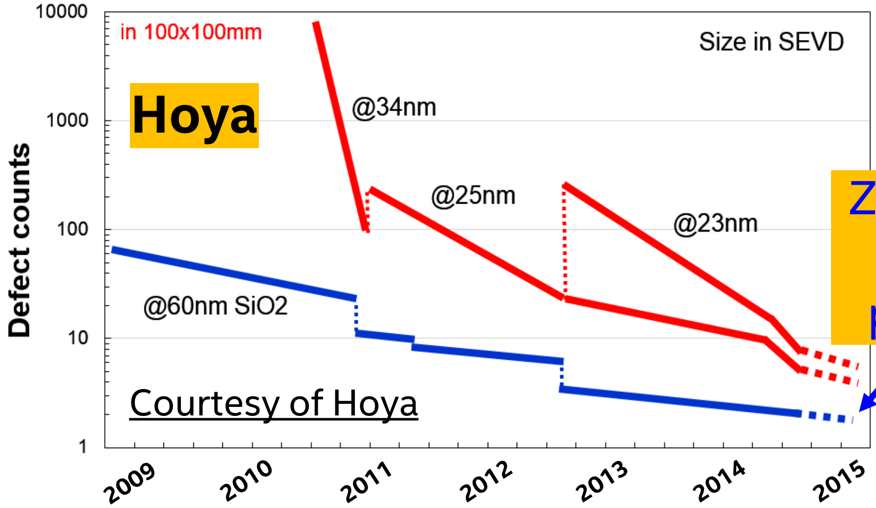
EUV infrastructure has 8 key programs

2 are ready or near-ready now, 5 are in development, 1 has significant gaps

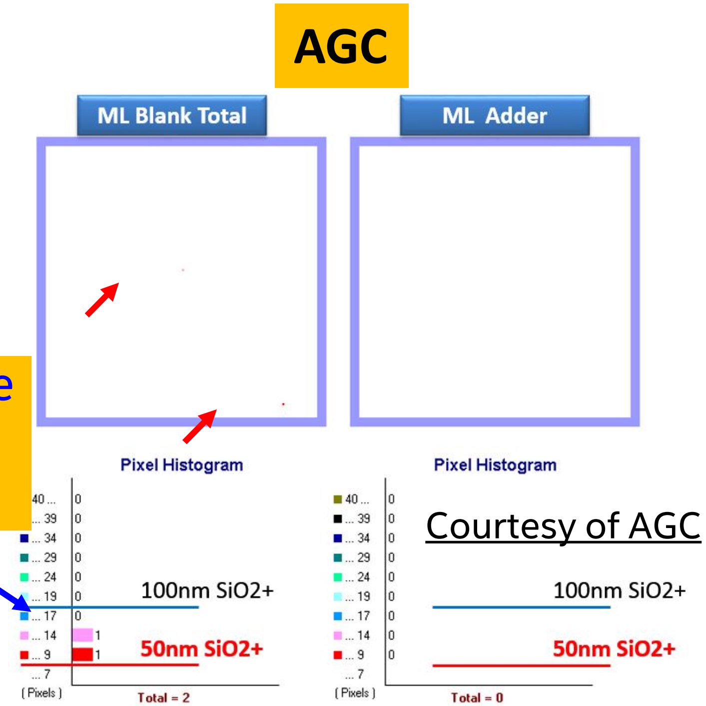
- **E-beam Mask Inspection:** In use for low volume production. Need TPT increase.
- **AIMS Mask Inspection:** Imaging demonstrated
- **Actinic Blank Inspection (ABI):** Ready for qualification of HVM quality blanks in ‘16
- **Pellicle:** ASML commercializing – production phase in 2H 2016
- **EUV blank quality:** Process and yield improvements ongoing
- **Actinic Patterned Mask Inspection (APMI):** High resolution PWI for fab. Still need actinic inspection in mask shop.
- **Blank multi-layer deposition tool:** Improving defect results. Multiple deposition techniques being evaluated to define HVM tool approach.
- **EUV resist QC:** QC center at IMEC expected online in 2017

EUVL mask blank ML defect trend

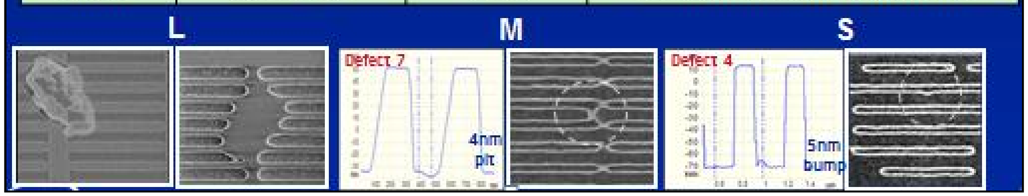
- Blank quality continues to improve
  - Defect # in single digit on best blanks
  - Large defects mostly eliminated on quality blanks



Zero large defects possible



Bin	Relative Size	Impact	Goal : Solution
Large	> hp	Killer	Elimination
Medium	≈ hp to ½ hp	Killer to ΔCD	Elimination + reduction : Mitigation
Small	≈ < ½ hp	ΔCD	Reduction : Compensation



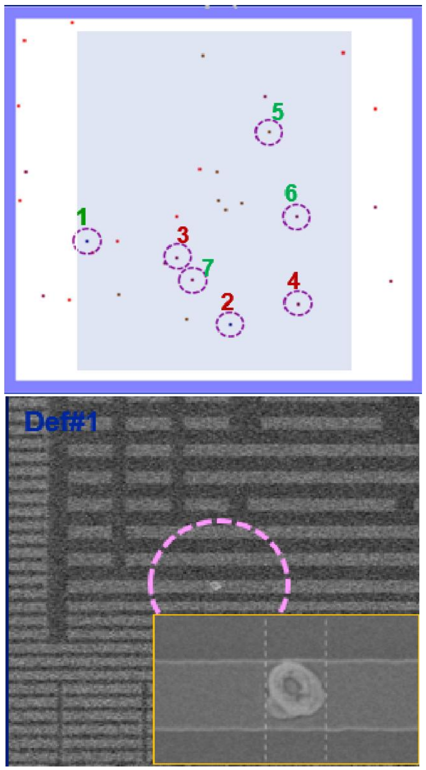
Analysis presented at EUV Symp 2011, still true today

- Blank quality for patterning tighter pattern layers
  - Eliminate ML defects > hp; difficult to covered by absorber
  - Reduce ML phase defects; become printable, require actinic blank inspection

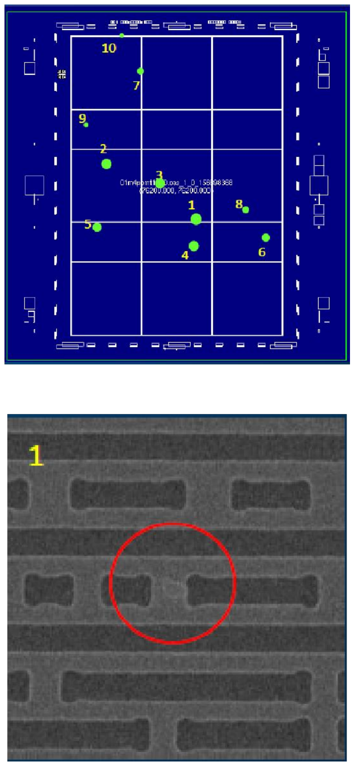
Foil from Ted Liang (Intel) et al. BACUS 2015, Monterey, California, USA, 9/29/2015

Mitigation demonstrated on multiple devices

- Many defects can be mitigated
- More defects can be covered on a dark field mask



7 mitigated
(22nm device, BF)



10 mitigated
(14nm device, DF)

- **Mitigation flow**
  - Blanks with fiducials
  - Sort and pair blank with specific pattern layer
  - Pattern shift computations
    - These two steps require fast data automation
  - During write: accurate alignment
  - After patterning: AIMS verification
  - Defect compensation repair

Foil from Ted Liang (Intel) et al. BACUS 2015, Monterey, California, USA, 9/29/2015

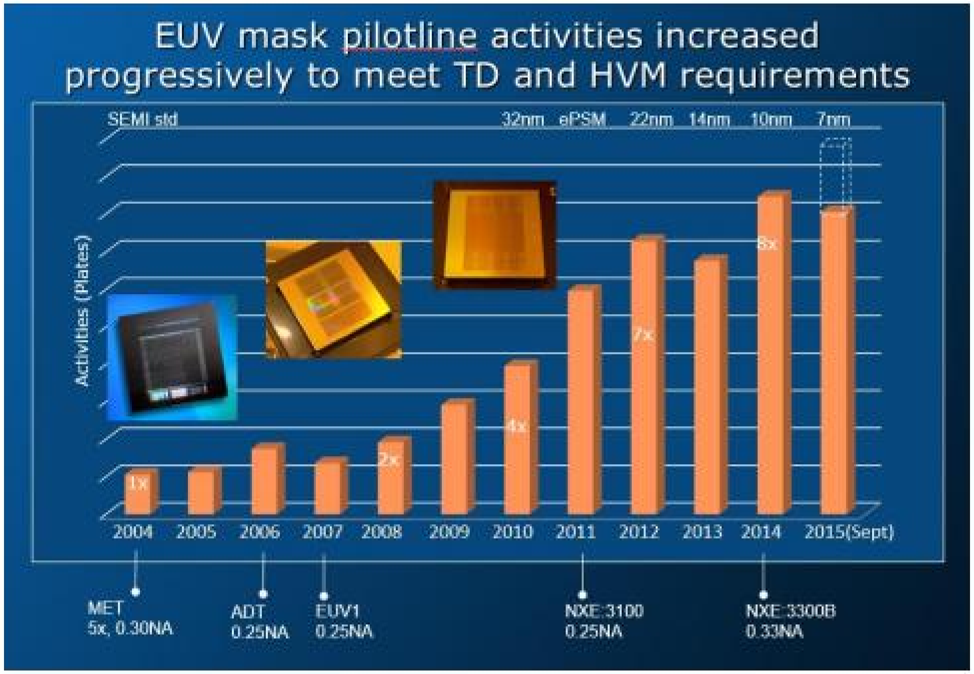
From 2015 iEUVLS

Bottom line: N7 mask with no printing defects

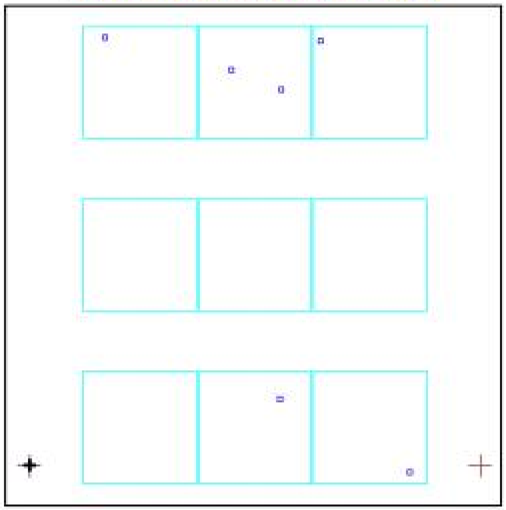
Progress in EUV Mask Fabrication

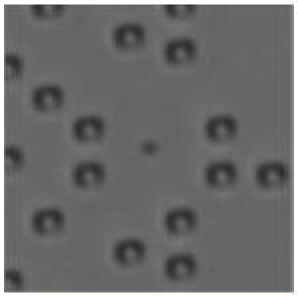
- Demonstrated feasibility to deliver EUV masks in quantity and quality to support EUVL development

~10X increase over 10 years



An N7 VIA test mask





All the 6 defects shown are non-printable

Guojing Zhang/Intel, 2014 BACUS (updated)

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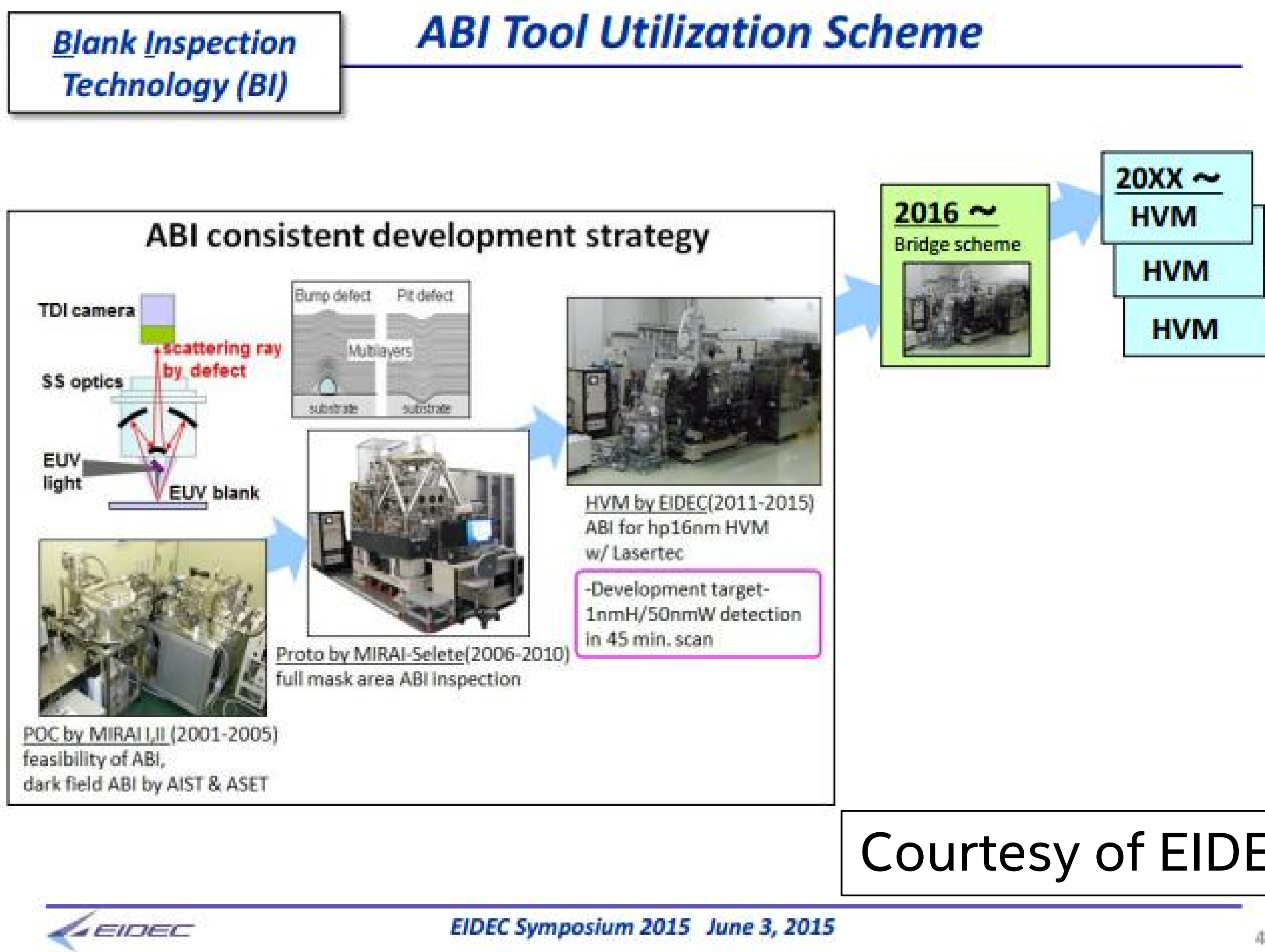
BACUS SPIE Photomask Sept. 29, 2015, Monterey, CA

ABI will be available for qualification of HVM quality blanks from Apr'16

Intel is an EIDEC (industry consortia in Japan) program member for advancing ABI technology.

- ABI is a critical tool for inspection of pit and bump phase defects on mask blanks.
- The ABI tool will be available for qualification of HVM quality blanks from Apr '16 onwards.
- Further hardware upgrades in 2016 will enable better resolution and overlay metrology



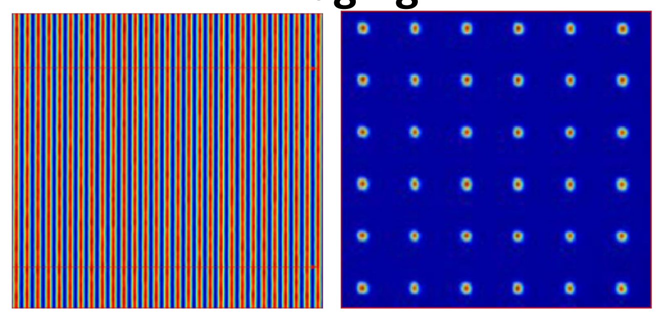
Courtesy of EIDEC

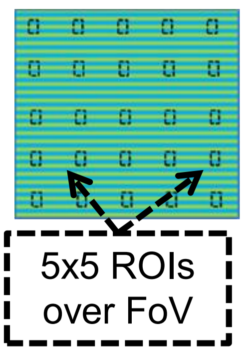
EUV AIMS

- System in calibration and qualification phase
  - To date, most complex/expensive EUV mask tool
- Imaging and run-rate are in-spec
  - Imaging contrast
  - CD reproducibility (champion), better than 1.6nm
  - Run-rate, 43 sites/hr
- Tasks ahead
  - Final system integration: environmental control, SW automation
  - Delivery to customers

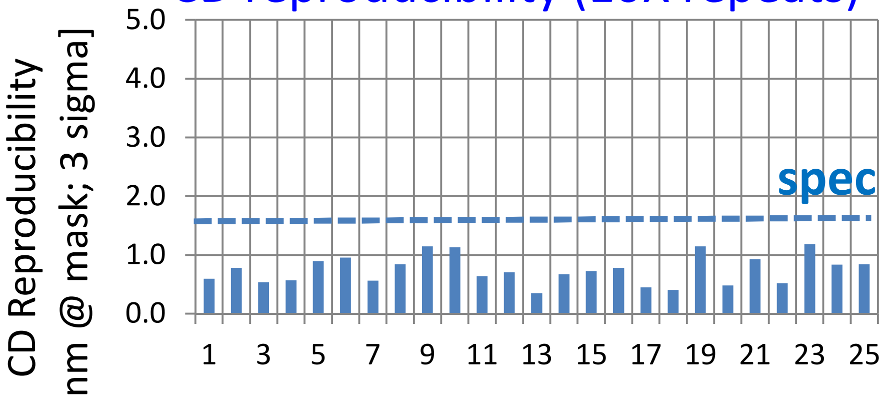
AIMS™ EUV Prototype

Imaging



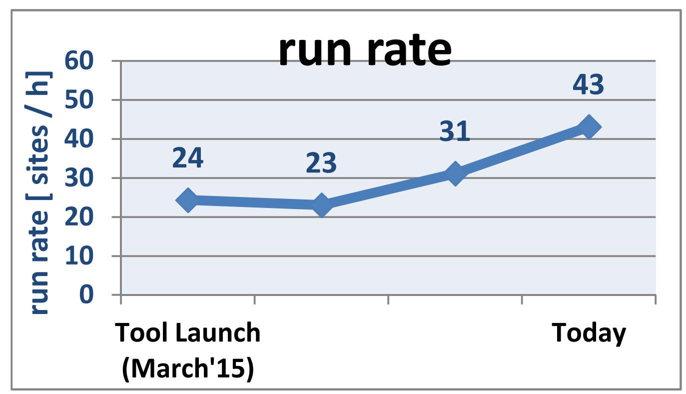


CD reproducibility (10X repeats)



25 measurement sites

Courtesy of Carl Zeiss



Foil from Ted Liang (Intel) et al. BACUS 2015, Monterey, California, USA, 9/29/2015

Excerpt from 2015 BACUS

Post-pellicle mask qualification

- Direct qualification with thru-pellicle inspection (TPI) in mask shop
  - The industry standard, the only known effective way to guarantee integrity of a pattern under pellicle (particle adders, contamination, PID)
  - Optical inspection is not feasible (low transmission, long wavelengths)
  - Actinic pattern mask inspection (APMI) is only way; However, APMI will not be ready in time to intercept EUV insertion due to long development time
- APMI development needs to start now and occur in parallel with EUV introduction
- For long term, TPI is needed to directly monitor what happens to mask patterns without removing the pellicle
  - Detect PID-like contamination on mask surface before impacting wafer yield
  - Increase productivity by avoiding the cycle of wafer print

Excerpt from Ted Liang (Intel) et al. foil BACUS 2015, Monterey, California, USA, 9/29/2015

EUV resist materials QC

- JSR & IMEC announced in May their partnership to enable manufacturing and QC of EUV resists open to all suppliers
- Partnership to be formalized by establishing a joint venture
    - JSR will provide manufacturing technology to the JV
    - IMEC to provide expertise and services to the JV for material QC
    - Services will be neutral and open to all suppliers
- Intel supports the formation of this JV for material qualification
- Intel recognizes the JV as a critical part of the EUV infrastructure that needs access by all that is both reliable and affordable
- Intel will continue to screen materials until the QC services are formally available, which is expected in early 2017

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- **EUV resist QC:** QC center at IMEC expected online in 2017

As presented at 2015 iEUVLS

Reticle defectivity

Front-side reticle defectivity: 10x reduction/year realized

ASML

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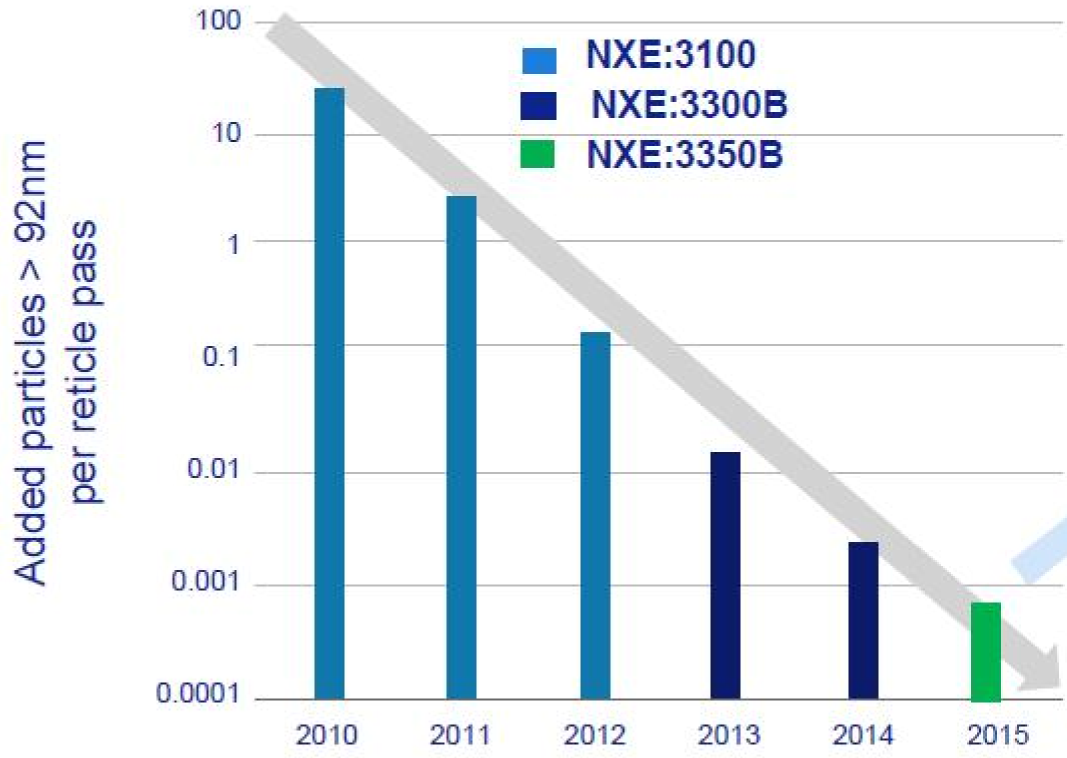
Slide 26
5 Oct 2015



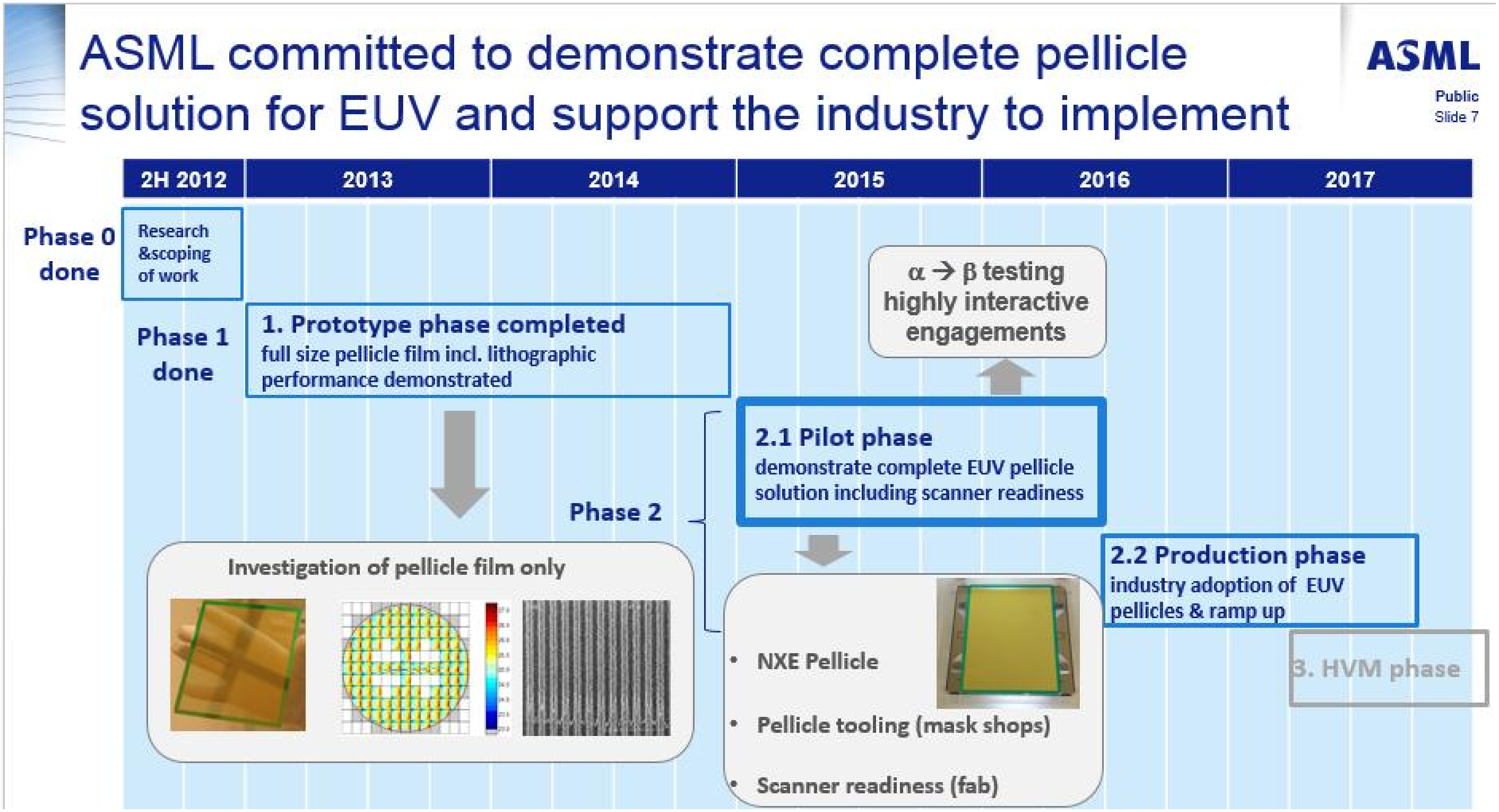
Test	# Cycles	# Added Particles	PRP Value
A	228	0	< 0.004
B	140	0	< 0.007
C	450	0	< 0.002
D	222	1	0.0045
E	133	0	< 0.007
Cumulative	**1173**	**1**	**0.0008**

Customer requirement for full production without pellicle

Source: Martin van den Brink (ASML) 2015 EUVL Symposium

- Scanner defectivity decreasing but not zero → Pellicle is Required

Complete pellicle solution



Slide courtesy ASML, October 2015

Pellicle Frame components and tooling

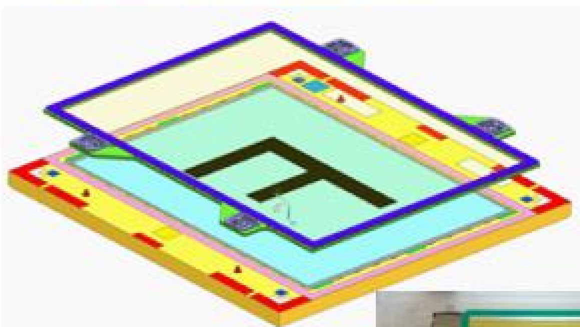
NXE pellicle frame components in manufacturing phase

All designs frozen, production of parts ongoing, first hardware coming in

Public
Slide 9

February '15:

- Initial design & first concept introduced
- First demonstrator built

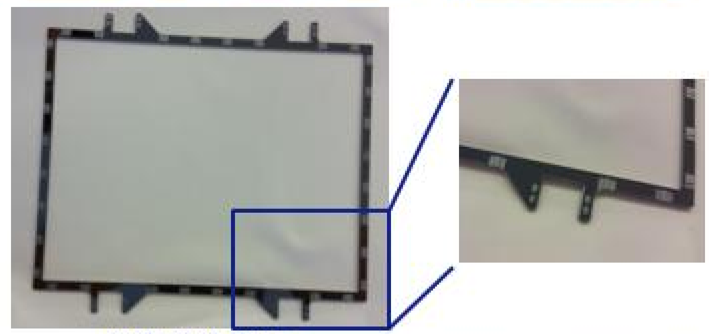


NXE pellicle concept

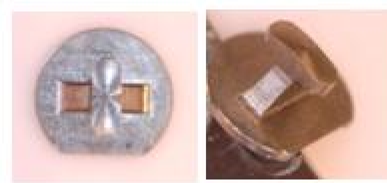
NXE pellicle demonstration model

September '15:

- Design optimized & finalized
- Pellicle frame parts being manufactured



Pellicle frame



Studs (interface to reticle)

Fixtures

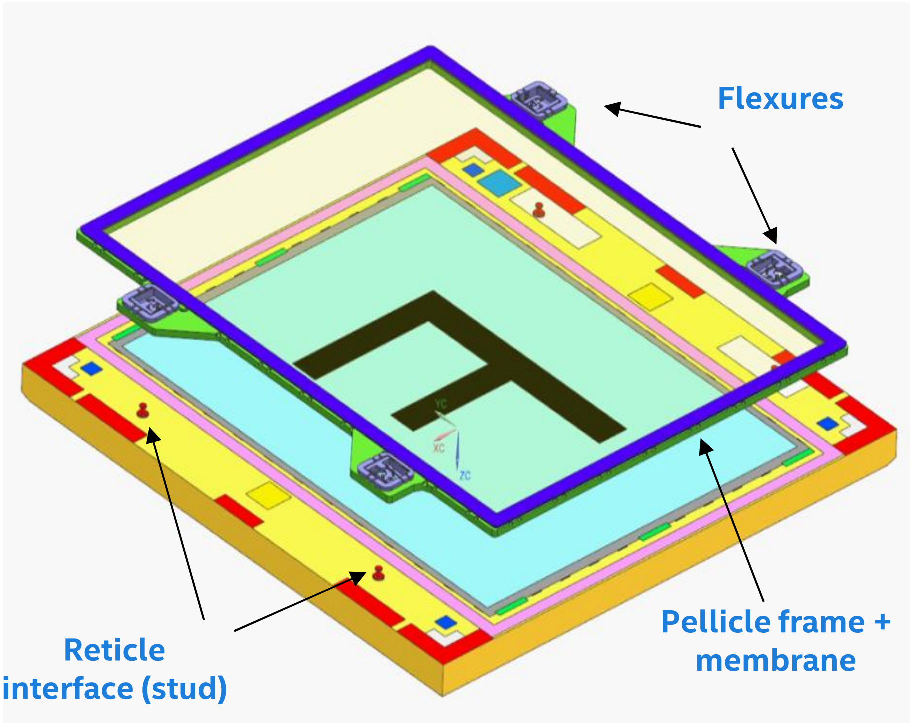
Slide courtesy ASML, October 2015

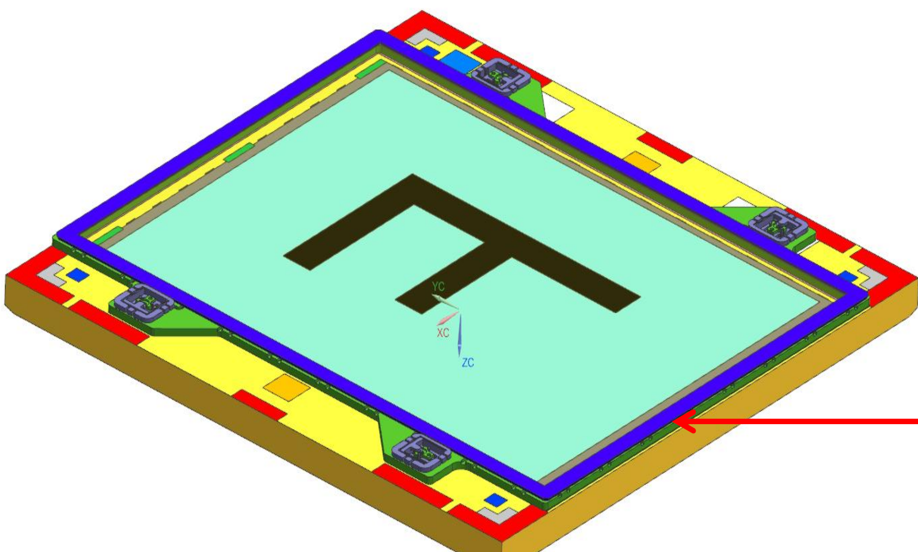
- Complete solution includes pellicle frame and membrane as well as mask shop tooling

Interchangeable NXE Pellicle concept

As presented at PMJ 2015

Allowing multiple inspection schemes





Key features

- Reticle front side defect-free solution
  - protects reticle front side from fall-on defects
  - particle free material combination and mounting technology to prevent particle generation
  - additional particle suppression towards pattern area
- Designed for use in NXE scanner
  - pump down/vent cycles compatible
  - vacuum and H_2 environment compatible
  - meets outgassing requirements
  - no overlay impact, distortion-free mounting
- Compatible with standard EUV mask flow
  - concept supports any type of pattern mask inspection: optical, e-beam, and actinic; both at mask shop and fab
  - allows for reticle repel cycle

1. **Pellicle frame is not sealed. 200um gap needed for pump-down**
2. **ASML simulation predicts 1/200 attenuation of small particles**
3. **Critical to verify!**

Slide courtesy ASML.

Gap verification in process…

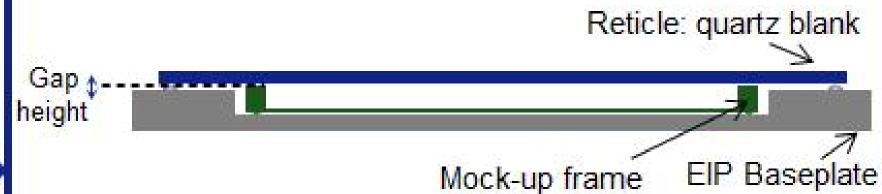
NXE pellicle integration in progress

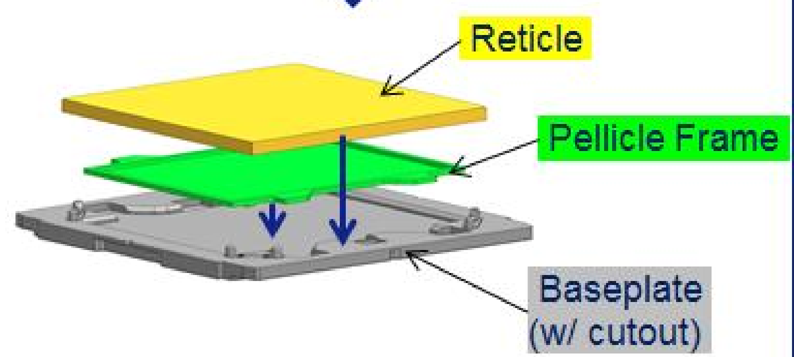
Early pellicle testing ongoing

ASML
Public
Slide 14

Integration testing	Status
Modified load lock – preliminary testing	Done
Scanner compatibility – preliminary testing	Done
Verify frame concept (200 µm gap)	In progress
Modified load lock for early access	In progress
Alpha testing load lock for early access	In progress

Frame mock-up used to verify 200 µm gap frame concept

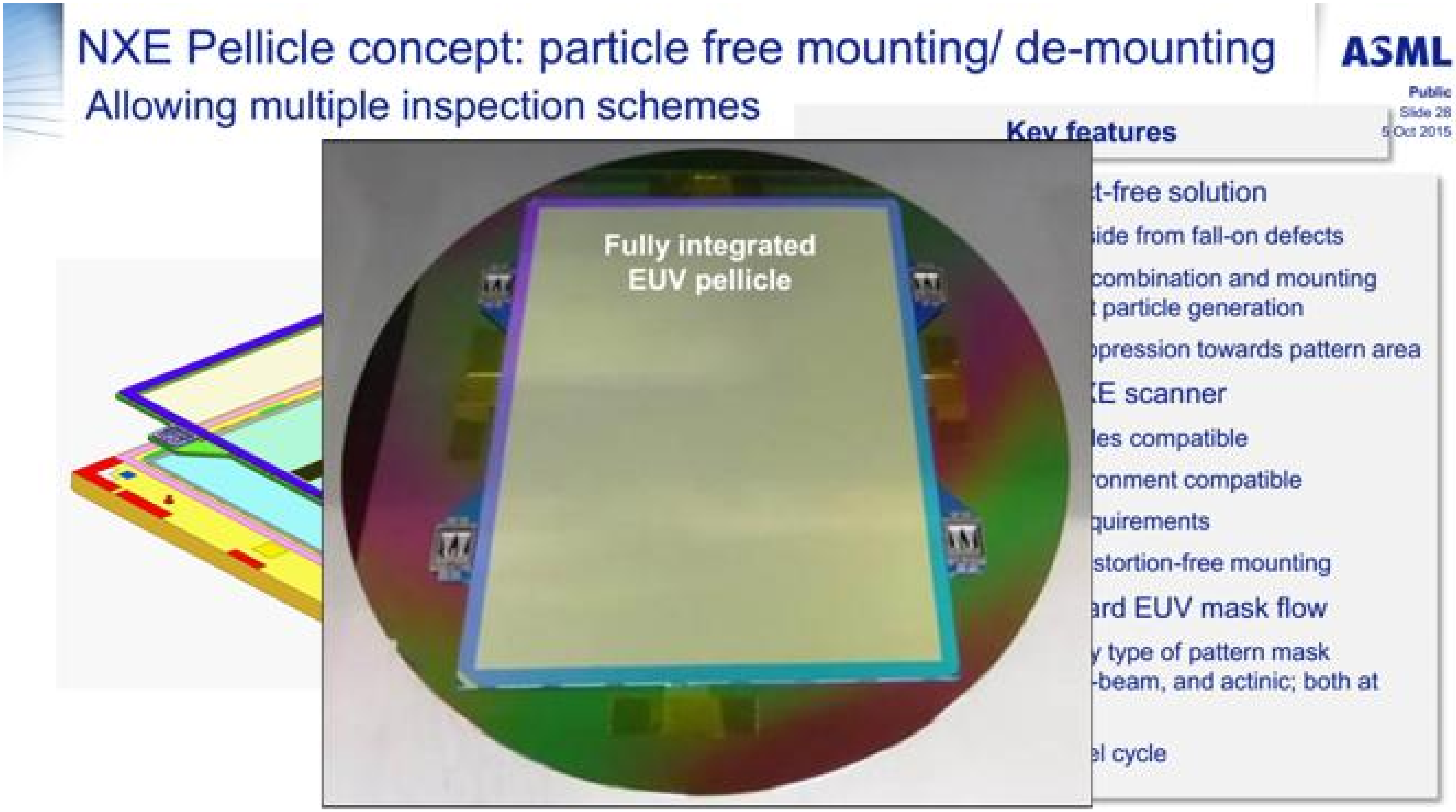




Mock-up frame

Slide courtesy ASML / Carmen Zoldesi, 2015 BACUS

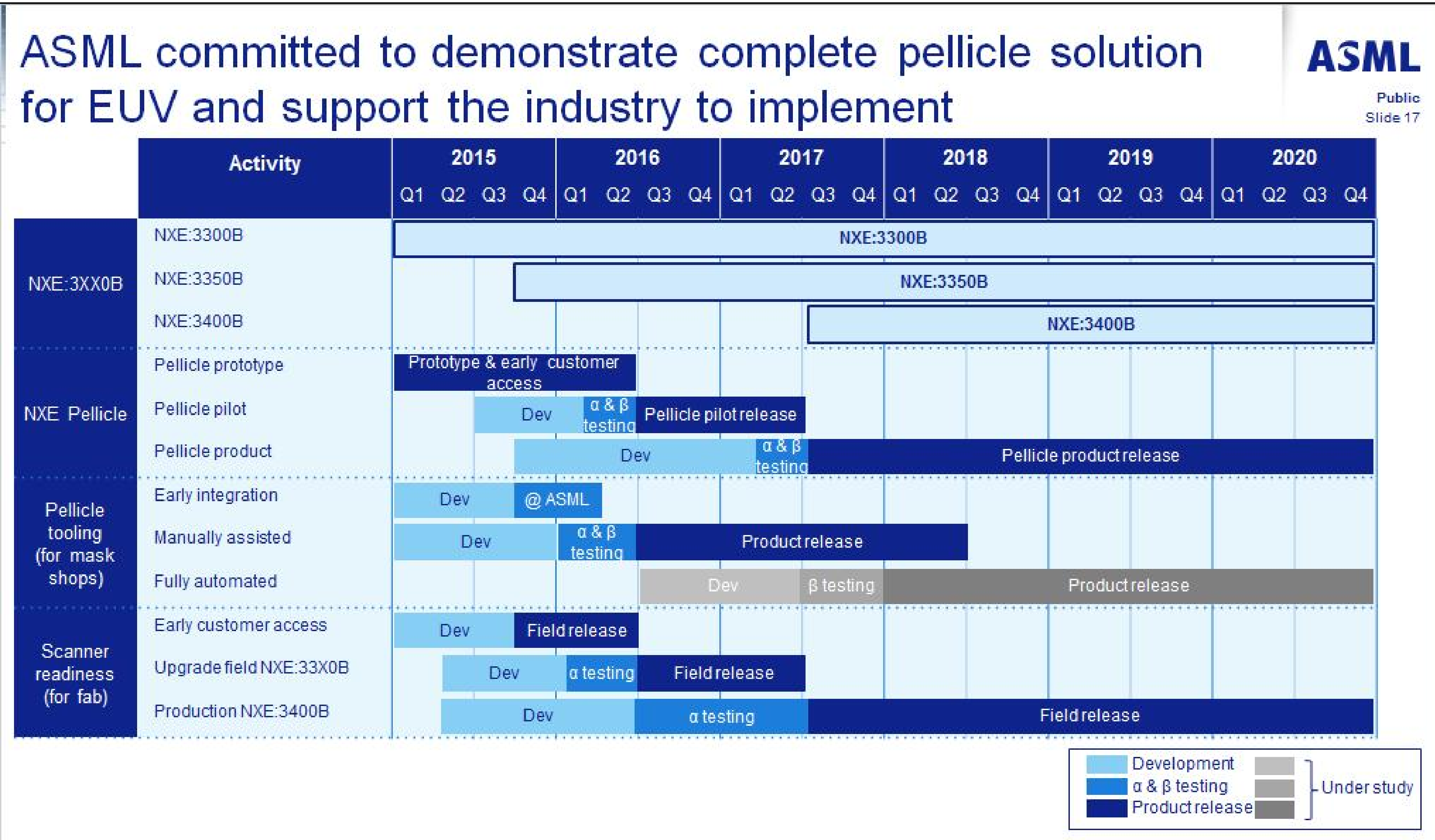
Full-size pellicle



Slide courtesy ASML, October 2015

- Active development by ASML and others

Commercialization timeline tight but OK



Slide courtesy ASML, October 2015

As of Today

Good progress on infrastructure in last year

Especially reticles, for example:

- N7 via mask with no printing defects
- Improved reticle pod qualified, and modified to support pelliclized masks
- ABI tool supporting blank manufacturers and mask shops, with a QC center to support qualification of HVM quality blanks starting in April 2016
- First fully integrated pellicle, and commercialization plan
- RBI qualification
- AIMS imaging demonstrated
- Champion blanks with no large defects and ~10 small defects (allows pattern shift mitigation)

Outline

- Recent historical trends
- Progress and remaining gaps
- EUVL infrastructure
- Next steps toward production

Scored as of today

What gates committing a process node to EUV?

- Technology Development requires rapid information turns
  - Availability: tool must be up to run TD wafers without delay – This is the critical, gating concern today
- HVM requires reasonable COO and predictability, driven by:
  - Productivity (mostly source power) – Good progress versus HVM need date
  - Availability (mostly source availability) – Long way to go, but making progress and have some time
  - OpEx (mostly source consumables) – Long way to go, but making progress and have some time
- HVM requires confidence in yield, driven by:
  - Mask blank defects and mitigation – Good progress versus HVM need date
  - Mask pattern defect (manufacturing and fall-on particles) detection – Need actinic solution

Conclusions

- Two years of solid progress on EUVL with nine 0.33NA systems shipped, generally meeting all performance requirements not related to source power
- Rapid proliferation and stable field performance in 80W config
- Combined availability ~60% with >15,000 good wafers patterned over eight week period
- Availability is adequate for process development. Need continued gains in availability to enable HVM insertion (meet 75% availability target in 2016).
- *In situ* collector cleaning looks promising, but needs to be delivered to field to gain confidence in OpEx and stable productivity
- Accelerated progress in source power over the past year lends credibility to source power roadmap. Matching productivity for High-NA requires ~2X increase in source power.
- EUV infrastructure making gains, e.g. mask blank
- Need actinic metrology source for pattern mask inspection in mask shop
- Enormous strides in pellicle development; need data on robustness and lifetime of membrane

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